and/or claims by the current Amendment. The attached page is captioned "**VERSIONS WITH MARKINGS TO SHOW CHANGES MADE**".

It is noted that the amendments are made only to more particularly define the invention and not for distinguishing the invention over the prior art, for narrowing the scope of the claims, or for any reason related to a statutory requirement for patentability.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and claimed (e.g., claim 1), is directed to an electrically conductive layer composed of a copper alloy, which includes at least one of Ag, As, Bi, P, Sb, Si and Ti at not less than 0.1 percent by weight.

Separately, the copper alloy can also include at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight as disclosed and claimed (e.g., claim 12).

Two key features are that the electrically conductive layer composed of the copper alloy has a melting point lower than copper and suppresses the mass-transfer of copper through the copper alloy. (See Page 13, lines 10-12; and Page 16, lines 10-21).

With the invention, the resultant composition, including the electrically conductive layer, the copper alloy has relatively large crystal grain sizes and reduced crystal grain boundaries in a current flow direction. Thus, a reduction in electromigration of an interconnection layer in a semiconductor device is produced decreasing the probability of disconnection and cracking of the interconnection layer, thereby improving the reliability and productivity of the semiconductor device.(See Page 54, lines 1-10).

II. THE PRIOR ART REJECTION

A. The § 103(a) Rejection Based on Tsuji, Edelstein et al., and Dubin

First, Applicant asserts that it would not have been obvious to combine, generally, three (3) references in this chemical patent case to show Applicant's invention. When prior art references require selective combination of specific elements to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight obtained from the invention itself. Accordingly, it clearly would not be obvious to one skilled in the art to combine the three cited references, and related specific elements, to produce Applicant's invention where the copper alloy has relatively large crystal grain sizes and reduced crystal grain boundaries in a current flow direction. Based on the structure of the copper alloy, Applicant's invention is designed to reduce electromigration of an interconnection layer in a semiconductor device by decreasing the probability of disconnection and cracking of the interconnection layer, thereby improving the reliability and productivity of the semiconductor device

In contrast, Tsuji et al. ("Tsuji") teaches copper foil for film carrier application. However, it does not teach a copper alloy improved for on-chip or off-chip wiring interconnections to meet the electromigration resistance and adhesion property requirements of new high capacity semiconductor chips. Tsuji, in particular, teaches a range of 0.05 - 0.2 weight % for various elements, including As and Si, where the percentages in this range make it difficult to obtain a sufficiently reduced melting point of the copper alloy as the copper alloy has relatively small crystal grain sizes and many crystal grain boundaries. (See Page 14, lines 1-17). By using a range of specific weight percentages instead of a minimum weight percent like Applicant, e.g., as indicated by the language "at least," this form re-enforces the assertion

that Tsuji does not teach or disclose decreasing the melting point of the copper alloy, and thus Tsuji does not teach being combined with any reference that would decrease the melting point of the copper alloy. (See MPEP 2144.05).

Compared to Tsuji, Applicant's invention produces an unexpected result as Applicant teaches the use of specific elements in the copper alloy of at least 0.1 percent by weight in order to reduce the melting point of the copper alloy below copper's melting point. Use of the copper alloy (e.g, as recited in claims 1 and 12) produces relatively large crystal grain sizes as well as crystal grain boundaries reduced in a current flow direction. Applicant recites the use of Mo, Ta or W for the purpose of increasing the grain boundaries.

Since Tsuji is not focused on producing larger crystal grain sizes and reduced crystal grain boundaries, Tsuji does not provide any teaching, disclosure or reason to further modify the copper alloy with the additional elements (disclosed above) in Applicant's Invention, or any other elements, from Edelstein, Dubin or any other reference. Therefore, Applicant's invention is patentable over this combination.

For emphasis, Tsuji and Edelstein ("Edelstein"), separately or in combination, fail to teach, disclose or provide a motivation for combining specifically identified copper alloys forming interface leads from Tsuji with specific copper alloys having the following elements: Bi, P, Sb, Ti, Mo, Ta and W, used to form electrically conductive layers embedded within semiconductor circuits, independent of any range, from Edelstein, or combined in the manner suggested to produce Applicant's invention

Second, Applicant separately asserts that Applicant's invention recites that a key difference with the cited references is that the composition of the copper alloy includes at least one element of Ag, As, B, P, Sb, Si, and Ti not less than 0.1 percent by weight. Independently,

the composition of the copper alloy can also include at least one element of Mo, Ta, and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.

Accordingly, Applicant agrees with the Examiner's assertion that Tsuji et al. does not teach "all [of] the additives claimed."

Even if combined, arguendo only, Edelstein can not make up for the compositional deficiencies of Tsuji as discussed above. Edelstein recites a copper alloy seed layer formed from a copper alloy. The elements expressly identified to form the alloy, i.e., C, N, O, Cl or S are not the same elements, i.e., Ag, As, Bi, P, Sb, Si and Ti, used in Applicant's invention as defined in Claim 1. (See Columns 7 and 8, lines 64 - 4).

In addition, Edelstein recites a copper seed layer formed from a copper alloy where the elements expressly identified to form the alloy, i.e., Ta, Mo, W, Si, Ag and Ti, are elements used to form the copper alloy in Applicant's invention. (See Column 8, lines 33-44). However, Edelstein does not anywhere disclose, teach or suggest a percentage weight of any of these elements in the copper alloy but instead provides a thickness range of the copper seed layer, and thus Edelstein does not teach Applicant's percent weight range of not less than 0.1 percent weight to not more than 1 percent weight for an element in the alloy (e.g., as identified in Claim 12).

Edelstein's reference to the barrier layer being made from materials, which include Mo, Ta, W and related compounds (See Column 9, lines 29-31), fails to cite using these elements with copper as recited in Applicant's invention

Even if combined, arguendo only, Dubin can not make up for the compositional deficiencies of Tsuji and Edelstein. Dubin depicts a semiconductor device composed of various layers, including a seed layer 56, a diffusion barrier layer 52 and an adhesion

promoting layer. Each of these layers is formed from alloys. The seed layer 56 is formed from various copper alloys but the copper-silver (Cu-Ag) alloy is the only combination also found in Applicant's invention. (See column 5, line 66; column 6, lines 48-50; and column 7, lines 43-45). However, Dubin does not anywhere disclose, teach or suggest a percentage weight of the silver element, or any other element in the copper alloy, as depicted with Applicant's invention.

Dubin also depicts a diffusion barrier layer 52 composed a variety of element and alloys, in particular, Ta, Ta alloys, Wa, Wa alloys, Si or Ti and Ti alloys. However, none of these alloys are copper alloys as indicated in Claim 12 of Applicant's invention. This lack of using Cu is consistent with the diffusion barrier being used to provide additional protection against diffusion of Cu atoms from the Cu metallization through the dielectric layer 50. (See Column 7, lines 15-18).

Dubin further discloses an adhesion promoting layer 55 comprising materials such as Ta and Mo (See column 7, lines 37-40) but does not recite these materials as being used as elements of copper alloys.

Third, none of the above three layers are structurally similar to the structure of Applicant's invention.

Structurally, Applicant's invention recites an electrically conductive layer, i.e., copper-alloy interconnection, provided in an inter-layer insulator 10 on a semiconductor substrate of a semiconductor circuit. In particular, the inter-layer insulator 10 has a trench groove with a predetermined width where a barrier metal layer extends on a bottom and side walls of the trench groove of the inter-layer insulator so the copper alloy interconnection layer exists on the barrier metal layer (e.g., as defined by Claims 22 and 30). (See pages 52-53, lines 1-16; and

Figures 3A-3C).

Applicant disagrees with the Office Action and further asserts that Tsuji does not teach or suggest these structural features. Tsuji recites a film carrier having a resin base film 2 and a rolled copper foil laminated thereon with the rolled copper foil forming leads 3, 4 for mounting semiconductor chips or other electrical components in place. The rolled copper foil is made of a copper alloy composition. (See Column 3, lines 52-58). In particular, a film carrier with a base 2 is covered with a copper foil. The copper foil is photo-etched to provide copper inner leads 3 (fingers for chip bonding) and outer leads 4 (fingers for external connections) with testing pads 5. (See Column 1, lines 48-68). Both the inner leads 3 and outer leads 4 form an interface between external circuits and electrode terminals of a semiconductor chip. (See Column 1, lines 20-25; column 2, lines 8-17; and Figure 1). These leads are interfaces connected to the semiconductor chip but not physically embedded within a trench groove of a semiconductor circuit, and is completely unlike Applicant's invention. That is, Tsuji does not teach or suggest an electrically conductive layer embedded within a semiconductor circuit, independent of the particular material used.

Tsuji's structural features, therefore, are significantly different than Applicant's invention as noted above (e.g., as defined by Claim 1), and thus Tsuji fails to teach or suggest Applicant's invention independent of the type of material used to form these structural features. This Office Action has not identified any references which teach or suggest these structural components of Applicant's invention as noted above.

Edelstein uses copper alloys to form structures (and related functions) that are significantly different from Applicant's invention. In particular, Edelstein's copper alloy seed layer 78 are normally deposited under the main copper conductor layers 46, 56, 60 with the

seed layer 78 deposited over a barrier layer 72. (See Column 7, 1-32; and Figures 2-3D). This arrangement is structurally dissimilar from Applicant's electrically conductive layer composed of a copper alloy embedded within a trench groove of a semiconductor circuit where the electrically conductive layer is formed on a barrier layer, which is formed on an inter-layer insulator layer. As a result, there is no motivation to use a copper alloy from a seed layer located underneath a main conductive layer and use it for an electrically conductive layer as with Applicant's invention.

For emphasis, at a minimum, and independent of the composition of any copper alloy, Tsuji and Edelstein et al. ("Edelstein"), separately or in combination, structurally fail to teach, disclose, or provide a motivation for combining a rolled copper foil forming interface leads for mounting semiconductor chips or other electrical component from Tsuji with Edelstein's copper alloy seed layer 78 situated on a semiconductor substrate 52 to provide a base underneath a main conductor layer 46, 56, 60, 82, or combined in the manner suggested to produce Applicant's invention

Finally, regarding the dependent claims 2-11, 13-21, 23-29 and 31-37, which depend from claims 1, 12, 22 and 30, these claims are patentable not only by virtue of their dependency from the independent claim but also by the additional limitations they recite.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-37 and 57-63 all the claims presently pending in the application are patentably distinct over the prior art of record and are

in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 4/8/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

1. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of Ag, As, Bi, P, Sb, Si and Ti at not less than 0.1 percent by weight,

wherein said copper alloy has a melting point less than copper.

12. (Amended) An electrically conductive layer comprising:

a copper alloy which includes at least one of Mo, Ta, and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight,

wherein the mass-transfer of copper is suppressed through said copper alloy.

22. (Amended) A semiconductor device comprising:

a semiconductor substrate;

an insulation layer over said semiconductor substrate, and said insulation layer having a trench groove;

a barrier metal layer on a bottom and side walls of said trench groove; and

an electrically conductive layer provided in an interconnection layer on said barrier metal layer, and said interconnection layer filling said trench groove,

wherein said interconnection layer comprises a copper alloy which includes at least one of Ag, As, Bi, P, Sb, Si and Ti in a range of not less than 0.1 percent by weight to not more than a maximum solubility limit to copper, so that said copper alloy is in a solid solution.

30. (Amended) A semiconductor device comprising:

a semiconductor substrate;

an insulation layer over said semiconductor substrate, and said insulation layer having a trench groove;

a barrier metal layer on a bottom and side walls of said trench groove; and

an electrically conductive layer provided in an interconnection layer on said barrier metal layer, and said interconnection layer filling said trench groove,

wherein said interconnection layer comprises a copper alloy which includes at least one of Mo, Ta and W in a range of not less than 0.1 percent by weight to not more than 1 percent by weight.